PPU pin out and signal description

From Nesdev wiki

Pin out

Signal description

- R/W, CPU D0-D7, and CPU A0-A2, are signals from the CPU. CPU A2-A0 are tied to the corresponding CPU address pins and select the PPU register (0-7).
- /CS is generated by the 74139 (address decoder) on the mainboard to map the PPU regs in the CPU memory range from $2000 to $3FFF.
- EXTx allows the combination of two PPUs - setting the "slave" bit in the PPUCTRL ($2000) register causes the PPU to output palette indices to these pins, and clearing said bit causes it to instead read indices from these pins (and use them to select the background color).
    - For the Vs. System and Playchoice PPUs, EXT0…2 are replaced with R, G, and B respectively. EXT3 is tied to ground; its functionality is unknown.
- CLK is the 21.47727 MHz (NTSC) or 26.6017 MHz (PAL) clock input. It is doubled for the color generator (and then divided by 12 to get the colorburst frequency) and also divided by 4 (NTSC) or 5 (PAL) for the pixel and memory clocks.
- /INT is connected to the CPU's /NMI pin.
- ALE (Address Latch Enable) goes high at the beginning of a PPU VRAM access and is used to latch the lower 8 bits of the PPU's address bus; see the PPU address bus section of PPU rendering. It stays high for one PPU cycle.
- PPU ADx (Address + Data) is the PPU's data bus, multiplexed with the lower 8 bits of the PPU's address bus.
- PPU A8-A13 are the top 6 bits of the PPU's address bus.
- /RD and /WR specify that the PPU is reading from or writing to VRAM. As an exception, writing to the internal palette range (3F00-3FFF) will not assert /WR.
- /RST resets certain parts of the chip to their initial power-on state: the clock divider, video phase generator, scanline/pixel counters, and the even/odd frame toggle. It also keeps several registers zeroed out for a full frame: PPUCTRL, PPUMASK ($2001), PPUSCROLL ($2005; the VRAM address latch "T", fine X scroll, and the H/V toggle), and the VRAM read buffer. It is used in the NES to clear the screen when the console is

reset either by the button or the CIC, and in a dual-PPU system it can be used to genlock the two PPUs together.
- VOUT is the shifted analog video output. For the Vs. System and Playchoice PPUs, this is only the composite sync signal.

See also

- Wiring diagram of RF Famicom
- 電子機器(Electronics) Junker's redrawn schematic of the HVC-001 (http://green.ap.teacup.com/junker/116.html)
- Electronix Corp's redrawn schematic of the NES-001 (http://console5.com/wiki/Nintendo_NES-001#Schematics)
    - Note: Minor error on page "NES 3" for the power led / reset switch board: pin 5 connects to LED, pin 4 connects to switch, pin 3 is +5V.